Docket No.: 60188-028

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :
:
Toshio YAMADA :
:
Serial No.: :
(Divisional of Serial No. 09/102,166) : Group Art Unit:
:
Filed: February 09, 2001 : Examiner:
:
For: SEMICONDUCTOR INTEGRATED CIRCUIT, COMPUTER SYSTEM, DATA PROCESSOR AND DATA PROCESSING METHOD

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, DC 20231

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

IN THE CLAIMS:

Please amend claims 14 and 15 as follows:

14. (Amended) The computer system [,the data processor or the data processing method] of Claim [1, 2, 3 , 4 ,] 5[, 10, 12 or 13],

wherein said memory network has a bus network structure.

15. (Amended) The computer system [,the data processor or the data processing method] of Claim [1, 2, 3 , 4 ,] 5[, 10, 12 or 13],

wherein said memory network has a ring network structure.

Please add new claims 19-22 as follows:

--19. The data processor of Claim 12,

wherein said memory network has a bus network structure.

20. The data processor of Claim 12,

wherein said memory network has a ring network structure.

21. The data processing method of Claim 10 or 13,

wherein said memory network has a bus network structure.

22. The data processing method of Claim 10 or 13,

wherein said memory network has a ring network structure.--

REMARKS

Applicants request entry of the foregoing amendments prior to examination of the above-identified application. No new matter has been added.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 MEF:dtb
Date: February 9, 2001
Facsimile: (202) 756-8087